Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A random number generator comprising:

a plurality of groups of independent flip-flops, at least some of the groups having different connection configurations,

an exclusive-or (XOR) network connected to all of the outputs of the plurality of groups of flip-flops, wherein a metastable output of at least one flip-flop of the plurality of groups of flip-flops causes a random signal to be output by the XOR network for number generation, and

a latch connected to the output of the XOR network.

2. (original) The random number generator according to claim 1, wherein the groups of flip-flops are divided into at least three equally-sized groups.

3. (previously presented) The random number generator according to claim 1, wherein a first group of flip-flops comprises a first pair of cross-connected NAND gates without any buffers connected to first data and clock input lines,

wherein a second group of flip-flops comprises a second pair of cross-connected NAND gates with a first buffer connected to a second data input line of at least one NAND gate of the second pair of NAND gates; and

wherein a third group of flip-flops comprises a third pair of cross-connected NAND gates with a second buffer connected to a second clock input line of at least one NAND gate of the third pair of NAND gates.

4. (previously presented) The random number generator according to claim 1, wherein a first group of flip-flops comprises a first pair of cross-connected NAND gates without any buffers connected within a cross connection between the first pair of NAND gates, and

wherein a second group of flip-flops comprises a second pair of cross-connected NAND gates with a delay buffer connected within a cross connection between the NAND gates of the second pair of the NAND gates.

5. (previously presented) The random number generator according to claim 1, wherein a first group of flip-flops comprises a first pair of cross-connected NAND gates without any load connected to either of the NAND gates,

wherein a second group of flip-flops comprises a second pair of cross-connected NAND gates with a first capacitive load connected to a data input line of at least one NAND gate of the second pair of NAND gates, and

wherein a third group of flip-flops comprises a third pair of cross-connected NAND gates with a second capacitive load connected to a clock input of at least one NAND gate of the third pair of NAND gates.

6. (previously presented) The random number generator according to claim 5, wherein at least one capacitive load of the first and second capacitive loads comprises a multi-input gate.

7. (previously presented) The random number generator according to claim 1, wherein the groups of flip-flops comprise unequal numbers of flip-flops in each group.

8. (previously presented) The random number generator according to claim 1, wherein delay devices connected within each of the groups of flip-flops have different delay values.

9. (currently amended) The random number generator according to claim 1, wherein at least some of the flip-flops comprise NAND gates ~~are~~ implemented with Boolean equivalents of NAND gates.

10. (previously presented) The random number generator according to claim 1, wherein the groups of flip-flops are arranged into one of thirds or fifths.

11. (previously presented) A method for random number generation, comprising

providing a plurality of groups of independent flip-flops, at least some of the groups having different connection configurations,

connecting each of the outputs of the plurality of groups of flip-flops to an exclusive-or (XOR) network, wherein a metastable output of at least one of flip-flops causes a random signal to be output by the XOR network, and

connecting a latch to the output of the XOR network to receive the random signal output by the XOR network for random number generation.

12. (previously presented) The method according to claim 11, wherein providing the plurality of independent flip-flops further comprises:

arranging the groups of flip-flops into three equally-sized groups.

13. (previously presented) The method according to claim 11, wherein a first group comprises a first pair of cross-connected NAND gates without any buffers connected to first data and clock input lines,

wherein a second group comprises a second pair of cross-connected NAND gates with a first buffer connected to a second data input line of at least one NAND gate of the second pair of NAND gates; and

wherein a third group comprises a third pair of cross-connected NAND gates with a second buffer connected to a second clock input line of at least one NAND gate of the third pair of NAND gates.

14. (previously presented) The method according to claim 11, wherein a first group comprises a first pair of cross-connected NAND gates without any buffers connected within a cross connection between the first pair of NAND gates, and

wherein a second group comprises a second pair of cross-connected NAND gates with a delay buffer connected within a cross connection between the NAND gates of the second pair of NAND gates.

15. (previously presented) The method according to claim 11, wherein a first group comprises a first pair of cross-connected NAND gates without any load connected to either of the NAND gates,

wherein a second group comprises a second pair of cross-connected NAND gates with a first capacitive load connected to a data input line of at least one NAND gate of the second pair of NAND gates, and

wherein a third group comprises a third pair of cross-connected NAND gates with a second capacitive load connected to a clock input line of at least one NAND gate of the third pair of NAND gates.

16. (previously presented) The method according to claim 15, wherein at least one capacitive load of the first and second capacitive loads comprises a multi-input gate.

17. (previously presented) The method according to claim 11, wherein providing the plurality of groups of independent flip-flops further comprises arranging the groups of flip-flops to define groups with unequal numbers of flip-flops in each group.

18. (previously presented) The method according to claim 11, wherein each of the groups of flip-flops have different delay values.

19. (previously presented) The method according to claim 11, wherein providing the plurality of groups of independent flip-flops comprises providing NAND gates and Boolean equivalents of NAND gates.

20. (previously presented) The method according to claim 11, wherein the groups of flip-flops are arranged into one of thirds or fifths.